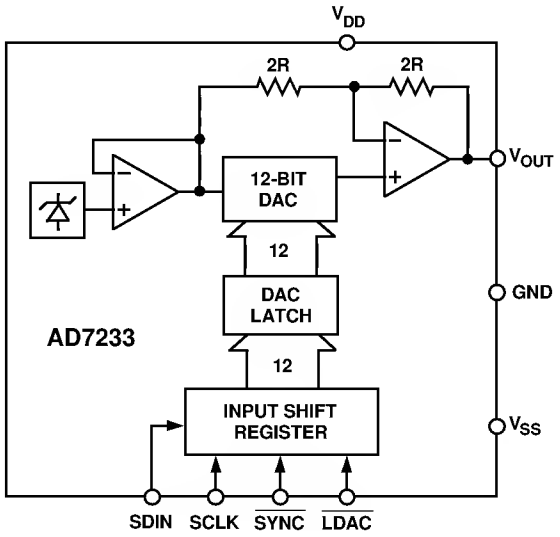
LC²MOS 12-Bit Serial Mini-DIP DACPORT

AD7233

FEATURES
12-Bit CMOS DAC with
On-Chip Voltage Reference
Output Amplifier
–5 V to +5 V Output Range
Serial Interface
300 kHz DAC Update Rate
Small Size: 8-Pin Mini-DIP
Nonlinearity: ±1/2 LSB T_{MIN} to T_{MAX}
Low Power Dissipation: 100 mW typ

APPLICATIONS
Process Control
Industrial Automation
Digital Signal Processing Systems
Input/Output Ports

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7233 is a complete 12-bit, voltage-output, digital-to-analog converter with output amplifier and Zener voltage reference all in an 8-pin package. No external trims are required to achieve full specified performance. The data format is 2s complement, and the output range is –5 V to +5 V.

The AD7233 features a fast, versatile serial interface which allows easy connection to both microcomputers and 16-bit digital signal processors with serial ports. When the $\overline{SYNC}$ input is taken low, data on the SDIN pin is clocked into the input shift register on each falling edge of SCLK. On completion of the 16-bit data transfer, bringing $\overline{LDAC}$ low updates the DAC latch with the lower 12 bits of data and updates the output. Alternatively, $\overline{LDAC}$ can be tied permanently low, and in this case the DAC register is automatically updated with the contents of the shift register when all sixteen data bits have been clocked in. The serial data may be applied at rates up to 5 MHz allowing a DAC update rate of 300 kHz.

For applications which require greater flexibility and unipolar output ranges with single supply operation, please refer to the AD7243 data sheet.

The AD7233 is fabricated on Linear Compatible CMOS (LC²MOS), an advanced, mixed-technology process. It is packaged in an 8-pin DIP package.

DACPORT is a registered trademark of Analog Devices, Inc.

PRODUCT HIGHLIGHTS

1. Complete 12-Bit DACPORT®.
2. The AD7233 is a complete, voltage output, 12-bit DAC on a single chip. This single-chip design is inherently more reliable than multichip designs.
3. Simple 3-wire interface to most microcontrollers and DSP processors.
4. DAC Update Rate—300 kHz.
5. Space Saving 8-Pin Package.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

AD7233–SPECIFICATIONS[1] (V_{DD} = +12 V to +15 V,[2] V_{SS} = –12 V to –15 V,[2] GND = 0 V, R_L = 2 kΩ, C_L = 100 pF to GND. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A	B	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	LSB max	
Differential Nonlinearity[3]	±0.9	±0.9	LSB max	Guaranteed Monotonic
Bipolar Zero Error[3]	±6	±6	LSB max	DAC Latch Contents 0000 0000 0000
Full-Scale Error[3]	±8	±8	LSB max	
Full-Scale Temperature Coefficient	±30	±30	ppm of FSR/°C typ	
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current				
I_{IN}	±1	±1	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance[4]	8	8	pF max	
ANALOG OUTPUTS				
Output Voltage Range	±5	±5	V	
DC Output Impedance	0.5	0.5	Ω typ	
AC CHARACTERISTICS[4]				
Voltage Output Settling Time				Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	10	10	μs max	Typically 3 μs; DAC Latch 100. . .000 to 011. . .111
Negative Full-Scale Change	10	10	μs max	Typically 5 μs; DAC Latch 011. . .111 to 100. . .000
Digital-to-Analog Glitch Impulse[3]	30	30	nV secs typ	DAC Latch Contents Toggled Between All 0s and all 1s
Digital Feedthrough[3]	10	10	nV secs typ	$\overline{LDAC}$ = High
POWER REQUIREMENTS				
V_{DD} Range	+10.8/+16.5	+11.4/+15.75	V min/V max	For Specified Performance Unless Otherwise Stated
V_{SS} Range	–10.8/–16.5	–11.4/–15.75	V min/V max	For Specified Performance Unless Otherwise Stated
I_{DD}	10	10	mA max	Output Unloaded; Typically 7 mA
I_{SS}	4	4	mA max	Output Unloaded; Typically 2 mA

NOTES
[1]Temperature Ranges are as follows: A, B Versions: –40°C to +85°C.
[2]Power Supply Tolerance: A Version: ±10%; B Version: ±5%.
[3]See Terminology.
[4]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +10.8 V to +16.5 V, V_{SS} = –10.8 V to –16.5 V, GND = 0 V, R_L = 2 kΩ, C_L = 100 pF. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Limit at +25°C (All Versions)	Limit at T_{MIN}, T_{MAX} (All Versions)	Units	Conditions/Comments
t_1[3]	200	200	ns min	SCLK Cycle Time
t_2	50	50	ns min	$\overline{SYNC}$ to SCLK Falling Edge Setup Time
t_3	120	190	ns min	$\overline{SYNC}$ to SCLK Hold Time
t_4	10	10	ns min	Data Setup Time
t_5	100	100	ns min	Data Hold Time
t_6	0	0	ns min	$\overline{SYNC}$ High to $\overline{LDAC}$ Low
t_7	50	50	ns min	$\overline{LDAC}$ Pulse Width
t_8	0	0	ns min	$\overline{LDAC}$ High to $\overline{SYNC}$ Low

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr and tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figure 3.
[3]SCLK Mark/Space Ratio range is 40/60 to 60/40.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... –0.3 V to +17 V
V_{SS} to GND ..... +0.3 V to –17 V
V_{OUT}[2] to GND ..... –6 V to V_{DD} +0.3 V
Digital Inputs to GND ..... –0.3 V to V_{DD} +0.3 V
Operating Temperature Range
  Industrial (A, B Versions) ..... –40°C to +85°C
  Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Power Dissipation to +75°C ..... 450 mW
Derates above +75°C by ..... 10 mW/°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]The output may be shorted to voltages in this range provided the power dissipation of the package is not exceeded. Short circuit current is typically 80 mA.

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Option*
AD7233AN	–40°C to +85°C	±1 LSB	N-8
AD7233BN	–40°C to +85°C	±1/2 LSB	N-8

*N = Plastic DIP.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7233 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

RELATIVE ACCURACY (LINEARITY)

Relative accuracy, or endpoint linearity, is a measure of the maximum deviation of the DAC transfer function from a straight line passing through the endpoints of the transfer function. It is measured after allowing for zero and full-scale errors and is expressed in LSBs or as a percentage of full-scale reading.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB or less over the operating temperature range ensures monotonicity.

BIPOLAR ZERO ERROR

Bipolar zero error is the voltage measured at V_{OUT} when the DAC is loaded with all 0s. It is due to a combination of offset errors in the DAC, amplifier and mismatch between the internal gain resistors around the amplifier.

FULL-SCALE ERROR

Full-scale error is a measure of the output error when the amplifier output is at full scale (full scale is either positive or negative full scale).

DIGITAL-TO-ANALOG GLITCH IMPULSE

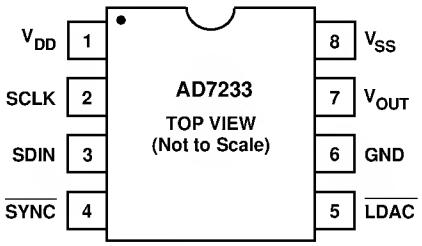
This is the voltage spike that appears at the output of the DAC when the digital code in the DAC latch changes before the output settles to its final value. The energy in the glitch is specified in nV secs, and is measured for an all codes change (0000 0000 0000 to 1111 1111 1111).

DIGITAL FEEDTHROUGH

This is a measure of the voltage spike that appears on V_{OUT} as a result of feedthrough from the digital inputs on the AD7233. It is measured with $\overline{LDAC}$ held high.

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	V_{DD}	Positive Supply (+12 V to +15 V).
2	SCLK	Serial Clock, Logic Input. Data is clocked into the input register on each falling SCLK edge.
3	SDIN	Serial Data In, Logic Input. The 16-bit serial data word is applied to this input.
4	$\overline{SYNC}$	Data Synchronization Pulse, Logic Input. Taking this input low initializes the internal logic in readiness for a new data word.
5	$\overline{LDAC}$	Load DAC, Logic Input. Updates the DAC output. The DAC output is updated on the falling edge of this signal, or alternatively if this line in permanently low, an automatic update mode is selected whereby the DAC is updated on the 16th falling SCLK pulse.
6	GND	Ground Pin = 0 V.
7	V_{OUT}	Analog Output Voltage. This is the buffered DAC output voltage (–5 V to +5 V).
8	V_{SS}	Negative Supply (–12 V to –15 V).



CIRCUIT INFORMATION

D/A Section

The AD7233 contains a 12-bit voltage-mode D/A converter consisting of highly stable thin-film resistors and high speed NMOS single-pole, double-throw switches.

Op Amp Section

The output of the voltage-mode D/A converter is buffered by a noninverting CMOS amplifier. The buffer amplifier is capable of developing ±5 V across a 2 kΩ load to GND.

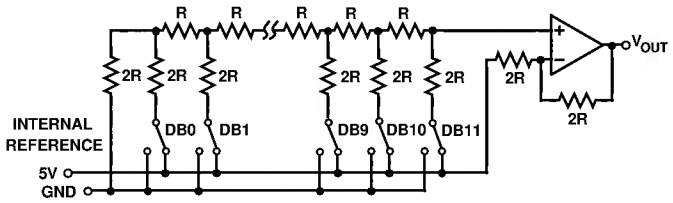


Figure 1. Simplified D/A Converter

DIGITAL INTERFACE

The AD7233 contains an input serial to parallel shift register and a DAC latch. A simplified diagram of the input loading circuitry is shown in Figure 2. Serial data on the SDIN input is loaded to the input register under control of $\overline{SYNC}$ and SCLK. When a complete word is held in the shift register it may then be loaded into the DAC latch under control of $\overline{LDAC}$. Only the data in the DAC latch determines the analog output on the AD7233.

A low $\overline{SYNC}$ input provides the frame synchronization signal which tells the AD7233 that valid serial data on the SDIN input will be available for the next 16 falling edges of SCLK. An internal counter/decoder circuit provides a low gating signal so that only 16 data bits are clocked into the input shift register. After 16 SCLK pulses the internal gating signal goes inactive (high) thus locking out any further clock pulses. Therefore, either a continuous clock or a burst clock source may be used to clock in the data.

The $\overline{SYNC}$ input should be taken high after the complete 16-bit word is loaded in.

Although 16 bits of data are clocked into the input register, only the latter 12 bits get transferred into the DAC latch. The first 4 bits in the 16-bit stream are don't cares since their value does not affect the DAC latch data. Therefore the data format is 4 don't cares followed by the 12-bit data word with the LSB as the last bit in the serial stream.

There are two ways in which the DAC latch and hence the analog output may be updated. The status of the $\overline{LDAC}$ input is examined after $\overline{SYNC}$ is taken low. Depending on its status, one of two update modes is selected.

If $\overline{LDAC}$ = 0 then the automatic update mode is selected. In this mode the DAC latch and analog output are updated automatically when the last bit in the serial data stream is clocked in. The update thus takes place on the sixteenth falling SCLK edge.

If $\overline{LDAC}$ = 1 then the automatic update is disabled and the DAC latch is updated by taking $\overline{LDAC}$ low any time after the 16-bit data transfer is complete. The update now occurs on the falling edge of $\overline{LDAC}$. This facility is useful for simultaneous update in multi-DAC systems. Note that the $\overline{LDAC}$ input must be taken back high again before the next data transfer is initiated.

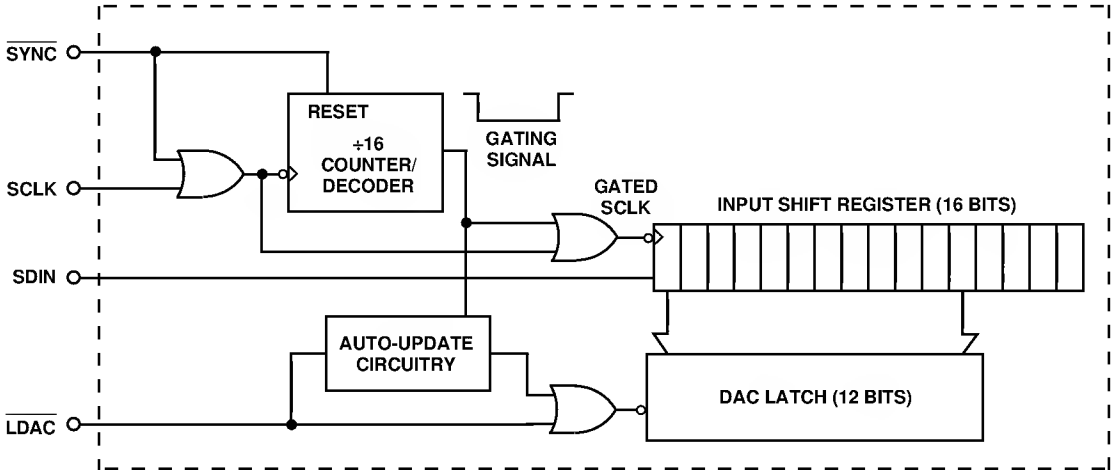


Figure 2. Simplified Loading Structure

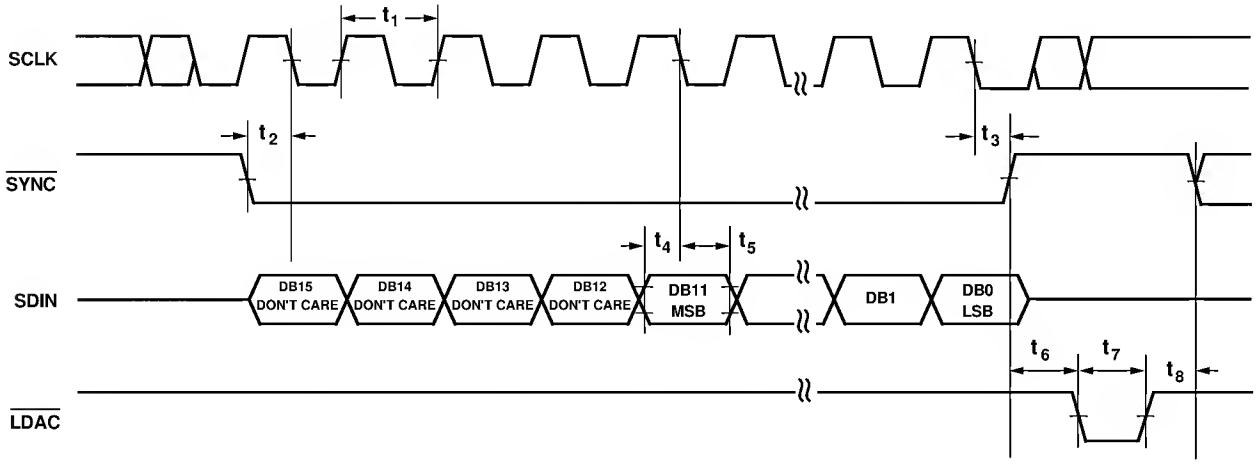
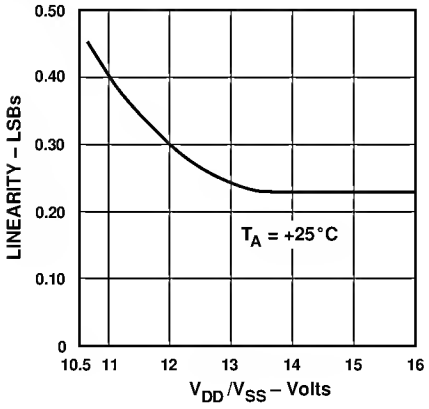
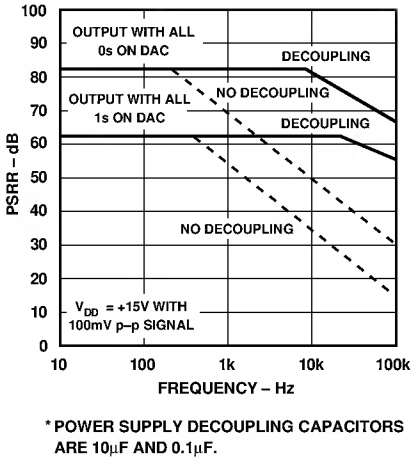


Figure 3. Timing Diagram

AD7233- Typical Performance Graphs

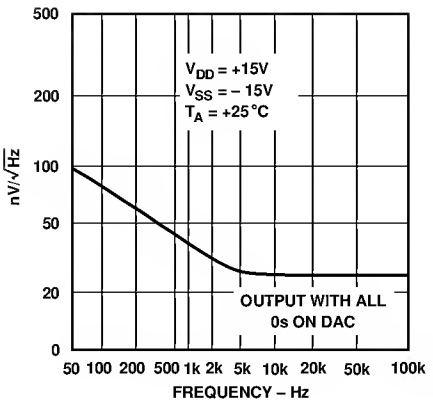


Linearity vs. Power Supply Voltage



* POWER SUPPLY DECOUPLING CAPACITORS ARE 10μF AND 0.1μF.

Power Supply Rejection Ratio vs. Frequency



Noise Spectral Density vs. Frequency

APPLYING THE AD7233

Bipolar (±5 V) Configuration

The AD7233 provides an output voltage range from –5 V to +5 V without any external components. This configuration is shown in Figure 4. The data format is 2s complement. The output code table is shown in Table I. If offset binary coding is required, then this can be done by inverting the MSB in software before the data is loaded to the AD7233.

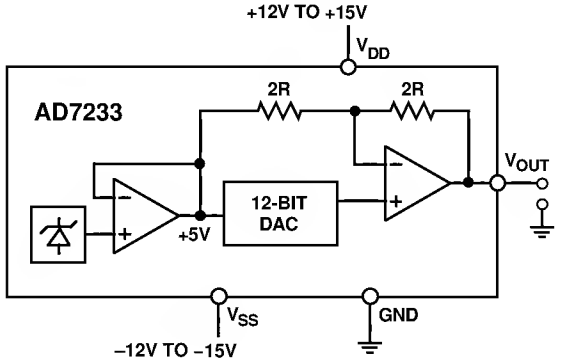


Figure 4. Circuit Configuration

Power Supply Decoupling

To achieve optimum performance when using the AD7233, the V_{DD} and V_{SS} lines should each be decoupled to GND using 0.1 μF capacitors. In very noisy environments it is recommended that 10 μF capacitors be connected in parallel with the 0.1 μF capacitors.

Table I. AD7233 Bipolar Code Table

Input Data Word MSB LSB	Analog Output, V_{OUT}
XXXX 0111 1111 1111	+5 V • (2047/2048)
XXXX 0000 0000 0001	+5 V • (1/2048)
XXXX 0000 0000 0000	0 V
XXXX 1111 1111 1111	–5 V • (1/2048)
XXXX 1000 0000 0001	–5 V • (2047/2048)
XXXX 1000 0000 0000	–5 V • (2048/2048) = –5 V

X = Don't Care
Note: 1 LSB = 5 V/2048 ≈ 2.4 mV

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD7233 is via a serial bus which uses standard protocol compatible with DSP processors and microcontrollers. The communications channel requires a three-wire interface consisting of a clock signal, a data signal and a synchronization signal. The AD7233 requires a 16-bit data word with data valid on the falling edge of SCLK. For all of the interfaces, the DAC update may be done automatically when all the data is clocked in or it may done under control of $\overline{\text{LDAC}}$.

Figures 5 to 8 show the AD7233 configured for interfacing to a number of popular DSP processors and microcontrollers.

AD7233–ADSP-2101/ADSP-2102 Interface

Figure 5 shows a serial interface between the AD7233 and the ADSP-2101/ADSP-2102 DSP processor. The ADSP-2101/ADSP-2102 contains two serial ports, and either port may be used in the interface. The data transfer is initiated by $\overline{\text{TFS}}$ going low. Data from the ADSP-2101/ADSP-2102 is clocked into the AD7233 on the falling edge of SCLK. When the data transfer is complete $\overline{\text{TFS}}$ is taken high. In the interface shown the DAC is updated using an external timer which generates an $\overline{\text{LDAC}}$ pulse. This could also be done using a control or decoded address line from the processor. Alternatively, the $\overline{\text{LDAC}}$ input could be hardwired low, and in this case the automatic update mode is selected whereby the DAC update takes place automatically on the 16th falling edge of SCLK.

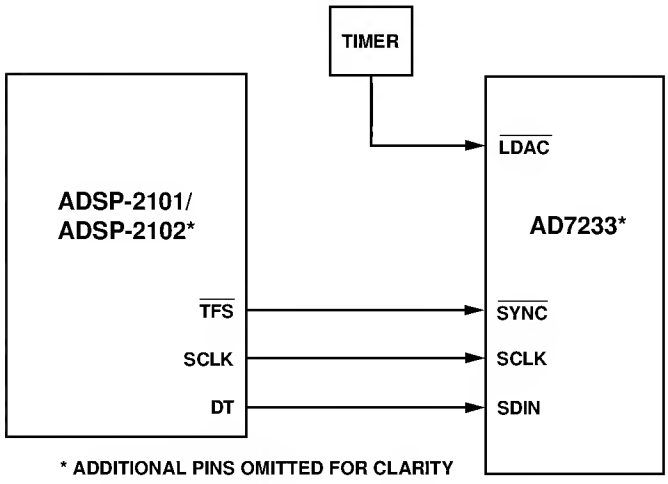


Figure 5. AD7233 to ADSP-2101/ADSP-2102 Interface

AD7233–DSP56000 Interface

A serial interface between the AD7233 and the DSP56000 is shown in Figure 6. The DSP56000 is configured for Normal Mode Asynchronous operation with Gated Clock. It is also set up for a 16-bit word with SCK and SC2 as outputs and the FSL control bit set to a 0. SCK is internally generated on the DSP56000 and applied to the AD7233 SCLK input. Data from the DSP56000 is valid on the falling edge of SCK. The SC2 output provides the framing pulse for valid data. This line must be inverted before being applied to the $\overline{\text{SYNC}}$ input of the AD7233.

The $\overline{\text{LDAC}}$ input of the AD7233 is connected to GND so the update of the DAC latch takes place automatically on the 16th falling edge of SCLK. An external timer could also be used as in the previous interface if an external update is required.

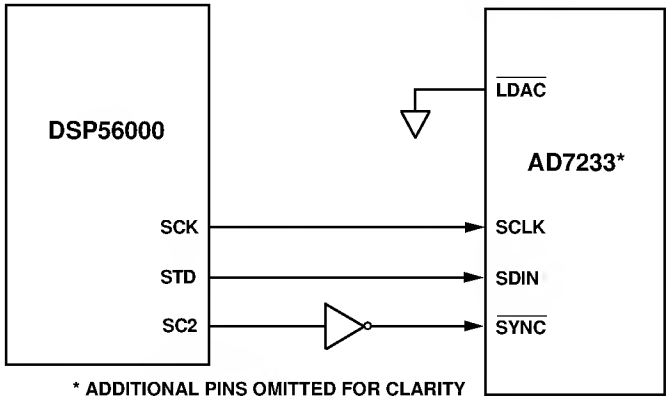


Figure 6. AD7233 to DSP56000 Interface

AD7233–87C51 Interface

A serial interface between the AD7233 and the 87C51 microcontroller is shown in Figure 7. TXD of the 87C51 drives SCLK of the AD7233 while RXD drives the serial data line of the part. The $\overline{\text{SYNC}}$ signal is derived from the port line P3.3.

The 87C51 provides the LSB of its SBUF register as the first bit in the serial data stream. Therefore, the user will have to ensure that the data in the SBUF register is arranged correctly so that the don't care bits are the first to be transmitted to the AD7233 and the last bit to be sent is the LSB of the word to be loaded to the AD7233. When data is to be transmitted to the part, P3.3 is taken low. Data on RXD is valid on the falling edge of TXD. The 87C51 transmits its serial data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7233, P3.3 is kept low after the first eight bits are transferred and a second byte of data is then transferred serially to the AD7233. When the second serial transfer is complete, the P3.3 line is taken high.

Figure 7 shows the $\overline{\text{LDAC}}$ input of the AD7233 hardwired low. As a result, the DAC latch and the analog output will be updated on the sixteenth falling edge of TXD after the $\overline{\text{SYNC}}$ signal for the DAC has gone low. Alternatively, the scheme used in previous interfaces, whereby the $\overline{\text{LDAC}}$ input is driven from a timer, can be used.

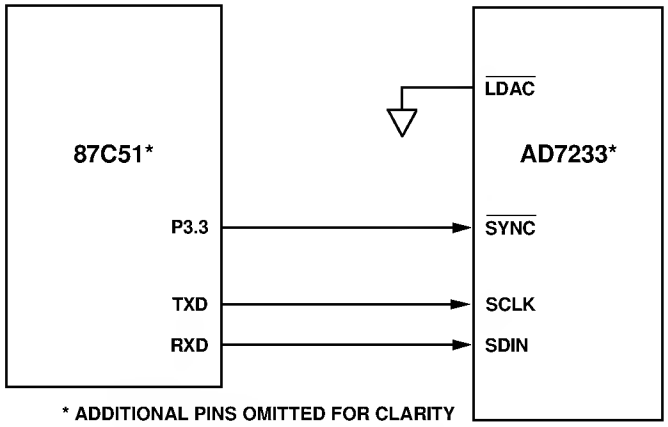


Figure 7. AD7233 to 87C51 Interface

AD7233-68HC11 Interface

Figure 8 shows a serial interface between the AD7233 and the 68HC11 microcontroller. SCK of the 68HC11 drives SCLK of the AD7233 while the MOSI output drives the serial data line. The $\overline{SYNC}$ signal is derived from a port line (PC7 shown).

For correct operation of this interface, the 68HC11 should be configured such that its CPOL bit is a 0 and its CPHA bit is a 1. When data is to be transmitted to the part, PC7 is taken low. When the 68HC11 is configured like this, data on MOSI is valid on the falling edge of SCK. The 68HC11 transmits its serial data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7233, PC7 is kept low after the first eight bits are transferred and a second byte of data is then transferred serially to the AD7233. When the second serial transfer is complete, the PC7 line is taken high. Figure 8 shows the $\overline{LDAC}$ input of the AD7233 hardwired low. As a result, the DAC latch and the analog output of the DAC will be updated on the sixteenth falling edge of SCK after the respective $\overline{SYNC}$ signal has gone low. Alternatively, the scheme used in previous interfaces, whereby the $\overline{LDAC}$ input is driven from a timer, can be used.

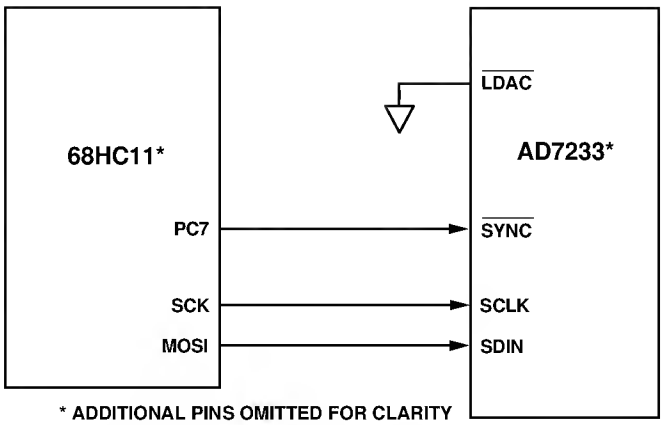


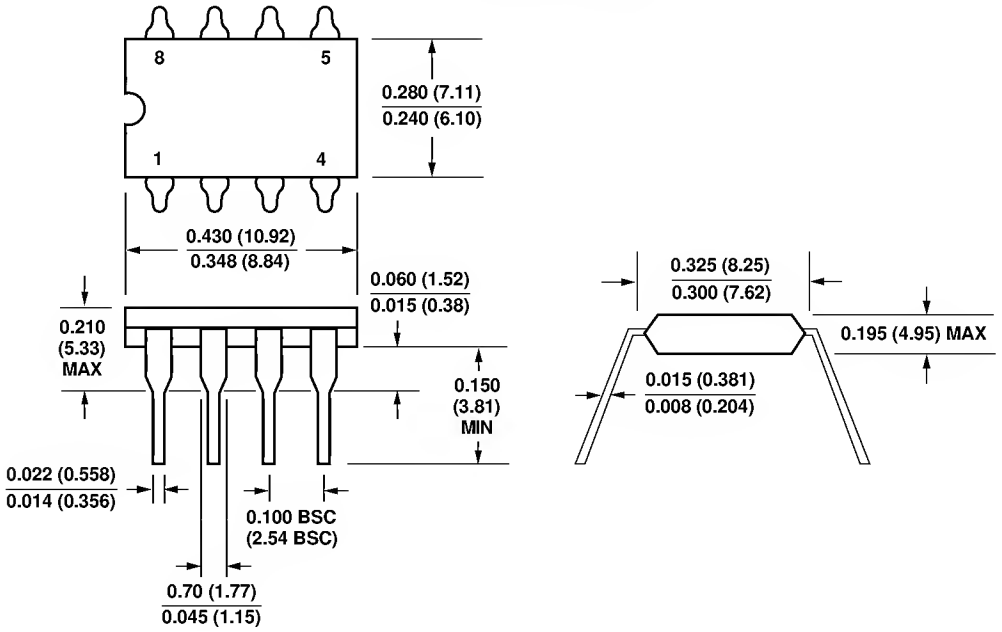
Figure 8. AD7233 to 68HC11 Interface

C1494–10–1/91

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Plastic DIP (N-8) Package



PRINTED IN U.S.A.